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APPLICANT : FUJITSU LTD;

INVENTOR : ITO MIKIO;

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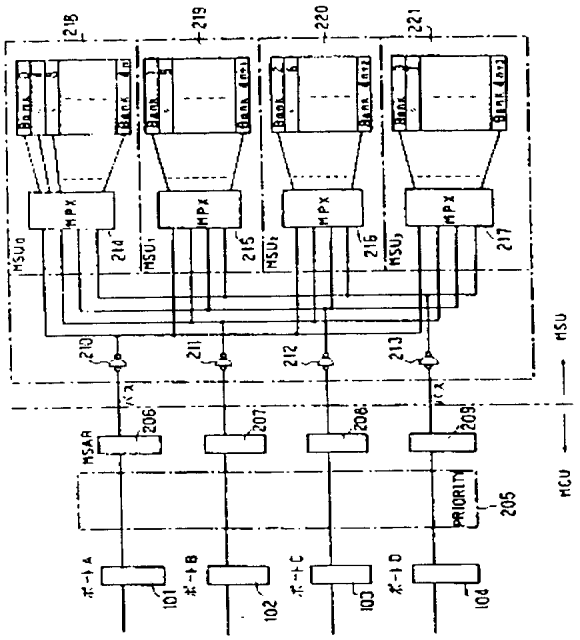
TITLE : MEMORY ACCESS CONTROL SYSTEM



ABSTRACT : PURPOSE: To prevent the occurrence of a bus contention by making a multiplexer perform an address supplying, and the output of the valid signals of a bank and a block to each bank according to an input address.

CONSTITUTION: The number of buses between a memory MSU and a memory controller MCU is the same as that of ports, and a multiplexer MPX is placed at each block in the MSU. A priority control circuit 205 checks only whether a memory access request at each port can be started up or not, and when it can be started up, it sets a request at a register MSAR, and transmits the memory access request to the MSU. The memory address registers MSAR 206~MSAR209 are used by all of the MSU blocks commonly, and are responded to each of the ports. The memory access request and the address set at the memory address register MSAR are sent to the MSU, and are branched with power gates 210~213, and are sent to memory blocks 218~221. Thereby, the memory access request from each port cannot compete with each other unless it is the access to the same bank.